UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/582,257	03/29/2007	Eiichi Takahashi	4082-75814-01	1325

24197 7590 03/15/2010

KLARQUIST SPARKMAN, LLP
121 SW SALMON STREET
SUITE 1600
PORTLAND, OR 97204

EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

MAIL DATE	DELIVERY MODE
03/15/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/582,257	TAKAHASHI ET AL.	
	Examiner	Art Unit	
	CHAT C. DO	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04/21/08; 03/29/07; 06/09/06;* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 June 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/09/06 and 04/21/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 8-10 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated, as addressed in the background art in pages 1-2. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claim 1 is objected to because of the following informalities:

Re claim 1, the applicant is advised to write out the term "FIR" as "Finite Impulse Response (FIR)" for clarification purposes.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morrow (U.S. 3,665,171) in view of Nakase et al. (U.S. 5,222,035).

Re claim 1, Morrow discloses in Figures 1-7 a FIR filter (e.g. abstract and Figure 7) comprising a plurality of input delay circuits (e.g. delay 10x in Figure 7) which are mutually connected in cascade and each of which delays the input data and outputs it (e.g. input the sample $x_k(nt)$ and output as delay corresponding samples in Figure 7) , and a plurality of multiplier circuits (e.g. multiplier 14x in Figure 7) each of which multiplies respective input data of said plurality of input delay circuit and the output data of the input delay circuit of the final stage by respective coefficients to make partial output data (e.g. coefficient Cx and output of multiplier 14x in Figure 7), and which sums up partial output data of said plurality of multiplier circuits to make filter output data (e.g. output of all summers 22x in Figure 7), wherein: said FIR filter comprises a plurality of element circuits which have one or more input delay circuits each of which is configured by dividing said plurality of input delay circuits mutually connected in cascade in the direction of the cascade (e.g. multiple set of elements in Figure 7 wherein each set comprises K sample delay, two multipliers and adder), and one or more multiplier circuits connected to said one or more input delay circuits (e.g. multipliers 14x in Figure 7), and which obtain partial sum data from partial output data of said one or more multiplier circuits (e.g. summer 22x in Figure 7), and among said plurality of element circuits, the initial stage element circuit outputs said partial sum data (e.g. first set of element comprises k sample delay 10(1), multipliers 14(0) and 14(1), and adder 22(1) in

Figure 7), and each of the succeeding element circuits from the second stage outputs the partial sum data obtained by adding said partial sum data obtained inside that element circuit to partial sum data output by the element circuit of the prior stage (e.g. other set of elements within Figure 7), and the element circuit of the final stage outputs the partial sum data as the filter output data (e.g. output of Figure 7).

Morrow fails to disclose (1) the initial stage element circuit output directly and (2) adding delayed partial sum data to the partial sum data output of prior stage. However, Nakase et al. disclose in Figures 15-19 (1) the initial stage element circuit output directly (e.g. first output of accumulation stage in Figure 302) and (2) adding delayed partial sum data to the partial sum data output of prior stage (e.g. by accumulating in component 302 wherein delay is achieved by the accumulation register 104 in Figure 15).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add (1) the initial stage element circuit output directly and (2) adding delayed partial sum data to the partial sum data output of prior stage as conceptually seen in Nakase et al.'s invention into Morrow's invention because it would enable to improve the system's performance (e.g. col. 1 lines 56-65).

Re claim 2, Morrow further discloses in Figures 1-7 characterized in that it comprises one initial stage element circuit which has one or more of said input delay circuits mutually connected in cascade into which filter input data is input (e.g. K sample delay 10x in Figure 7), and said one or more of said multiplier circuits each of which multiplies each of the input data of said one or more input delay circuits by respective coefficient to make partial output data (e.g. by the multiplier 14x correspondingly in

Figure 7), and a partial output adder which adds partial output data of said one or more multiplier circuits mutually to make partial sum data (e.g. clumping adder(s) 22x in Figure 7), one or more intermediate stage element circuits (e.g. any of the middle portion circuit of Figure 7) each of which has one or more of said input delay circuits mutually connected in cascade into which the output data of said initial stage element circuit or the output data from the final input delay circuit of said intermediate stage element circuit of the prior stage is input (e.g. K sample delay 10(2) and 10(3) in Figure 7), and said one or more of said multiplier circuits each of which multiplies each one of the input data from said one or more of said input delay circuits by respective coefficient to make partial output data (e.g. multipliers 14(2) and 14(3) in Figure 7), and a partial output adder which adds the partial output data from said one or more multiplier circuits mutually to make partial sum data (e.g. adders 22(2) and 22(3) in Figure 7), and a partial sum delay circuit which delays the partial sum data of said partial output adder (e.g. partial sum delay 20(3) in Figure 7), and a final stage element circuit (e.g. last stage of Figure 7) which has one or more of said plurality of input delay circuits mutually connected in cascade into which the output data from the final input delay circuit of said intermediate stage element circuit of the prior stage is input (e.g. K sample delay 10(4) and 10(5) in Figure 7), and said plurality of multiplier circuits each of which multiplies each one of the input data from one or more of said plurality of input delay circuits and the output data from the final stage of the input delay circuit by respective coefficient to make partial output data (e.g. multipliers 14(5) and 14(4) in Figure 7), and a partial output adder which adds the partial output data from said plurality of multiplier circuits mutually to make partial sum data, a

partial sum delay circuit which delays the partial sum data of said partial output adder (e.g. adders 22(4) and 22(5) and delay 20(5) in Figure 7).

Morrow fails to disclose a partial sum adder for intermediate and final stage which adds partial sum data delayed by said partial sum delay circuit and partial sum data of said initial stage element circuit or said intermediate stage element circuit of the prior stage to make partial sum data. However, Nakase et al. disclose in Figures 15-19 a partial sum adder for intermediate and final stage which adds partial sum data delayed by said partial sum delay circuit and partial sum data of said initial stage element circuit or said intermediate stage element circuit of the prior stage to make partial sum data (e.g. by the accumulator 302 in Figure 15).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a partial sum adder for intermediate and final stage which adds partial sum data delayed by said partial sum delay circuit and partial sum data of said initial stage element circuit or said intermediate stage element circuit of the prior stage to make partial sum data as conceptually seen in Nakase et al.'s invention into Morrow's invention because it would enable to improve the system's performance (e.g. col. 1 lines 56-65).

Re claim 3, Morrow further discloses in Figures 1-7 characterized in that it comprises a plurality of element circuit sets each of which corresponds to the respective one of a plurality of divided input data divided from the original filter input data, each element circuit set is composed of said initial stage element circuit, said intermediate stage element circuit, and said final stage element circuit, and among the plurality of

element circuit sets, said coefficients of said multiplier circuits of all the element circuits corresponding to the same stage are made equal (e.g. Cx in Figure 7), and it comprises a filter output adder which aligns the decimal points and sums up the partial output data as a filter output data output by said final stage element circuit of said plurality of element circuit sets, and outputs the filter output data having a bit length corresponding to that of the original input data (e.g. output of Figure 7).

Re claim 4, Morrow further discloses in Figures 1-7 characterized in that said coefficients of said multiplier circuits are variable (e.g. C is variable in Figure 7).

Re claim 5, Morrow further discloses in Figures 1-7 characterized in that it has one or more of said input delay circuits mutually connected in cascade (e.g. sample delay 10x in Figure 7), one or more of said multiplier circuits each of which multiplies each one of the input data from said one or more input delay circuits by respective coefficient to make partial output data (e.g. multipliers 14x in figure 7) and a partial output adder which adds the partial output data from said one or more multiplier circuits mutually to make partial sum data (e.g. adders 22x in Figure 7).

Re claim 6, Morrow further discloses in Figures 1-7 characterized in that it has one or more of said input delay circuits mutually connected in cascade (e.g. sample delay element 10x in Figure 7), one or more of said multiplier circuits each of which multiplies each one of the input data from said one or more input delay circuits by respective coefficient to make partial output data (e.g. multipliers 14x in Figure 7), a partial output adder which adds the partial output data from said one or more multiplier circuits mutually to make partial sum data (e.g. adders 22x in Figure 7), a partial sum delay

circuit which delays the partial sum data of said partial output adder (e.g. partial sum delay 20x in Figure 7).

Morrow fails to discloses in Figures 1-7 a partial sum adder which adds partial sum data delayed by said partial sum delay circuit and partial sum data of said initial stage element circuit or said intermediate stage element circuit of the prior stage to make partial sum data. However, Nakase et al. disclose in Figures 15-19 a partial sum adder which adds partial sum data delayed by said partial sum delay circuit and partial sum data of said initial stage element circuit or said intermediate stage element circuit of the prior stage to make partial sum data (e.g. by the accumulator 302 in Figure 15).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a partial sum adder which adds partial sum data delayed by said partial sum delay circuit and partial sum data of said initial stage element circuit or said intermediate stage element circuit of the prior stage to make partial sum data as conceptually seen in Nakase et al.'s invention into Morrow's invention because it would enable to improve the system's performance (e.g. col. 1 lines 56-65).

Re claim 7, Morrow further discloses in Figures 1-7 characterized in that it has one or more of said input delay circuits mutually connected in cascade (e.g. sample delay 10x in Figure 7), one or more of said multiplier circuits each of which multiplies the input data from said one or more input delay circuits the output data from the input delay circuit of the final stage by respective coefficient to make partial output data (e.g. multipliers 14x in Figure 7), a partial output adder which adds the partial output data from one or more of said multiplier circuits mutually to make partial sum data (e.g.

adders 22x in Figure 7), a partial sum delay circuit which delays the partial output data of said partial output adder (e.g. partial sum delay 20x in Figure 7).

Morrow fails to discloses in Figures 1-7 a partial sum adder which adds the partial sum data delayed by said partial sum delay circuit and the partial sum data of said intermediate stage element circuit of the prior stage to make filter output data. However, Nakase et al. disclose in Figures 15-19 a partial sum adder which adds the partial sum data delayed by said partial sum delay circuit and the partial sum data of said intermediate stage element circuit of the prior stage to make filter output data (e.g. by the accumulator 302 in Figure 15).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a partial sum adder which adds the partial sum data delayed by said partial sum delay circuit and the partial sum data of said intermediate stage element circuit of the prior stage to make filter output data as conceptually seen in Nakase et al.'s invention into Morrow's invention because it would enable to improve the system's performance (e.g. col. 1 lines 56-65).

Re claim 8, Morrow further discloses in Figures 1-7 characterized in that said element circuit for an FIR filter is substituted by at least one of said initial stage element circuit and said final stage element circuit (e.g. Figure 7 as minimum).

Re claim 9, Morrow further discloses in Figures 1-7 characterized in that said coefficients of said multiplier circuits are variable (e.g. C is variable in Figure 7).

Re claim 10, Morrow further discloses in Figures 1-7 characterized in that said coefficients of said multiplier circuits are variable (e.g. C is variable in Figure 7).

Re claim 11, Morrow further discloses in Figures 1-7 characterized in that it has one or more of said input delay circuits mutually connected in cascade, one or more of said multiplier circuits each of which multiplies each one of the input data from said one or more input delay circuits by respective coefficient to make partial output data (e.g. multipliers 14x in Figure 7), and a partial output adder which adds the partial output data from said one or more multiplier circuits mutually to make partial sum data (e.g. adders 22x in Figure 7).

Re claim 12, it has similar limitations as cited in claim 11. Thus, claim 12 is also rejected under the same rational as cited in the rejection of rejected claim 11.

Re claim 13, it has similar limitations as cited in claim 11. Thus, claim 13 is also rejected under the same rational as cited in the rejection of rejected claim 11.

Re claim 14, Morrow further discloses in Figures 1-7 characterized in that it has one or more of said input delay circuits mutually connected in cascade (e.g. sample delay 10x in Figure 7), one or more of said multiplier circuits each of which multiplies each one of the input data from said one or more input delay circuits by respective coefficient to make partial output data (e.g. multipliers 14x in Figure 7), a partial output adder which adds the partial output data from said one or more multiplier circuits mutually to make partial sum data (e.g. adders 22x in Figure 7), a partial sum delay circuit which delays the partial sum data of said partial output adder (e.g. partial sum delay 20x in Figure 7).

Morrow fails to discloses in Figures 1-7 a partial sum adder which adds partial sum data delayed by said partial sum delay circuit and partial sum data of said initial stage element circuit or said intermediate stage element circuit of the prior stage to make

partial sum data. However, Nakase et al. disclose in Figures 15-19 a partial sum adder which adds partial sum data delayed by said partial sum delay circuit and partial sum data of said initial stage element circuit or said intermediate stage element circuit of the prior stage to make partial sum data (e.g. by the accumulator 302 in Figure 15).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a partial sum adder which adds partial sum data delayed by said partial sum delay circuit and partial sum data of said initial stage element circuit or said intermediate stage element circuit of the prior stage to make partial sum data as conceptually seen in Nakase et al.'s invention into Morrow's invention because it would enable to improve the system's performance (e.g. col. 1 lines 56-65).

Re claim 15, it has similar limitations as cited in claim 14. Thus, claim 15 is also rejected under the same rational as cited in the rejection of rejected claim 14.

Re claim 16, it has similar limitations as cited in claim 14. Thus, claim 16 is also rejected under the same rational as cited in the rejection of rejected claim 14.

Re claim 17, Morrow further discloses in Figures 1-7 characterized in that it has one or more of said input delay circuits mutually connected in cascade (e.g. sample delay 10x in Figure 7), one or more of said multiplier circuits each of which multiplies the input data from said one or more input delay circuits the output data from the input delay circuit of the final stage by respective coefficient to make partial output data (e.g. multipliers 14x in Figure 7), a partial output adder which adds the partial output data from one or more of said multiplier circuits mutually to make partial sum data (e.g.

adders 22x in Figure 7), a partial sum delay circuit which delays the partial output data of said partial output adder (e.g. partial sum delay 20x in Figure 7).

Morrow fails to discloses in Figures 1-7 a partial sum adder which adds the partial sum data delayed by said partial sum delay circuit and the partial sum data of said intermediate stage element circuit of the prior stage to make filter output data. However, Nakase et al. disclose in Figures 15-19 a partial sum adder which adds the partial sum data delayed by said partial sum delay circuit and the partial sum data of said intermediate stage element circuit of the prior stage to make filter output data (e.g. by the accumulator 302 in Figure 15).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a partial sum adder which adds the partial sum data delayed by said partial sum delay circuit and the partial sum data of said intermediate stage element circuit of the prior stage to make filter output data as conceptually seen in Nakase et al.'s invention into Morrow's invention because it would enable to improve the system's performance (e.g. col. 1 lines 56-65).

Re claim 18, it has similar limitations as cited in claim 17. Thus, claim 18 is also rejected under the same rational as cited in the rejection of rejected claim 17.

Re claim 19, it has similar limitations as cited in claim 17. Thus, claim 19 is also rejected under the same rational as cited in the rejection of rejected claim 17.

Re claim 20, Morrow further discloses in Figures 1-7 characterized in that said coefficients of said multiplier circuits are variable (e.g. C is variable in Figure 7).

Re claim 21, Morrow further discloses in Figures 1-7 characterized in that said coefficients of said multiplier circuits are variable (e.g. C is variable in Figure 7).

Re claim 22, Morrow further discloses in Figures 1-7 characterized in that said coefficients of said multiplier circuits are variable (e.g. C is variable in Figure 7).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHAT C. DO whose telephone number is (571)272-3721. The examiner can normally be reached on Tue-Fri 9:00AM to 7:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chat C. Do/
Primary Examiner, Art Unit 2193

January 25, 2010